

## Silicon NPN Power Transistors

## 2N6058/2N6059

## DESCRIPTION

- With TO-3 package
- High gain
- High current
- High dissipation
- Complement to type 2N5883/2N5884

## APPLICATIONS

- They are intended for use in power linear and low frequency switching applications

## PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

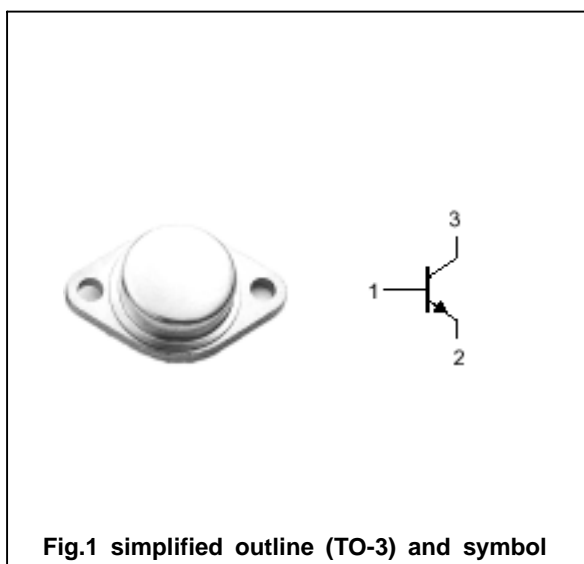


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings( $T_a =$ )

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	2N6058	80	V
		2N6059	100	
$V_{CEO}$	Collector-emitter voltage	2N6058	80	V
		2N6059	100	
$V_{EBO}$	Emitter-base voltage	Open collector	5	V
$I_C$	Collector current		12	A
$I_{CM}$	Collector current-peak		20	A
$I_B$	Base current		0.2	mA
$P_D$	Total Power Dissipation	$T_c=25$	150	W
$T_j$	Junction temperature		200	
$T_{stg}$	Storage temperature		-65~200	

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th-j-c}$	Thermal resistance junction to case	1.17	/W

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	
V <sub>CEO(sus)</sub>	Collector-emitter sustaining voltage	2N6058	I <sub>C</sub> =0.1A ; I <sub>B</sub> =0	80			V
		2N6059		100			V
V <sub>CEsat-1</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =6A I <sub>B</sub> =24mA			2	V	
V <sub>CEsat-2</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =12A I <sub>B</sub> =120mA			3	V	
V <sub>BEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =12A I <sub>B</sub> =120mA			4	V	
V <sub>BE</sub>	Base-emitter on voltage	I <sub>C</sub> =6A ; V <sub>CE</sub> =3V			2.8	V	
I <sub>CEO</sub>	Collector cut-off current	2N6058			1	mA	
		2N6059					V <sub>CE</sub> =50V; I <sub>B</sub> =0
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =5V; I <sub>C</sub> =0			2	mA	
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =6A ; V <sub>CE</sub> =3V	750				
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =12A ; V <sub>CE</sub> =3V	100				
f <sub>T</sub>	Transistion frequency	I <sub>C</sub> =5A ; V <sub>CE</sub> =3V; f=1MHz	4			MHz	

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PACKAGE OUTLINE

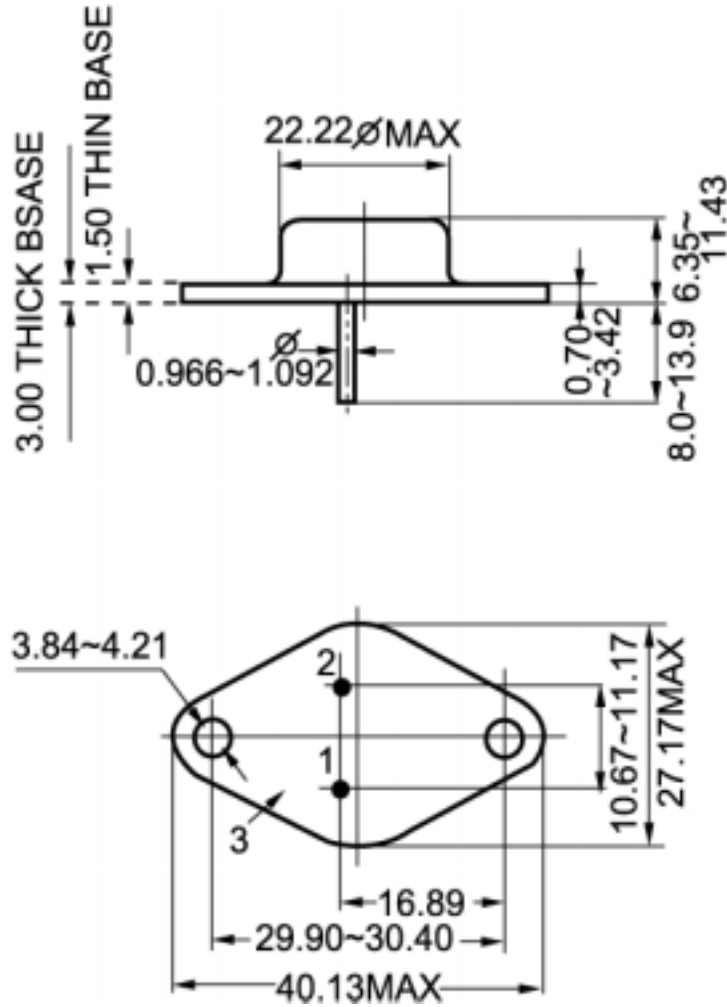


Fig.2 outline dimensions (unindicated tolerance: ± 0.10mm)