

Silicon PNP Power Transistors

2SA1063

DESCRIPTION

- With TO-3 package
- Low collector saturation voltage
- High transition frequency

APPLICATIONS

- Designed for general purpose switching and amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

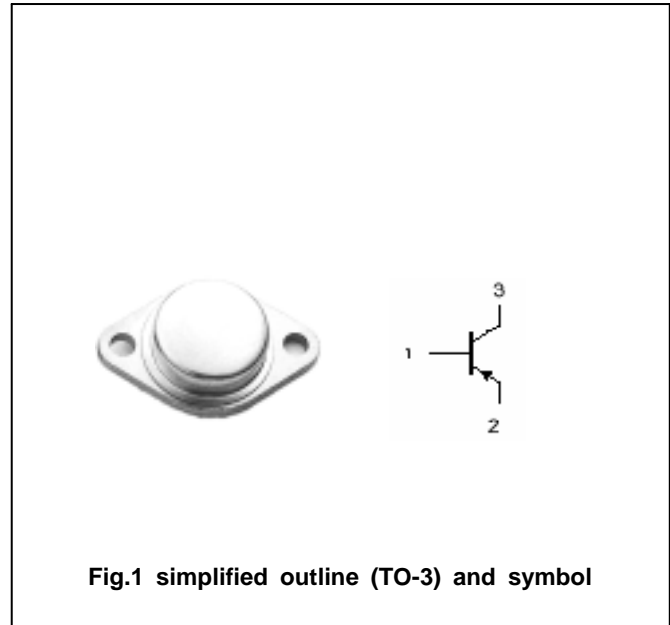


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a =$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-150	V
V_{CEO}	Collector-emitter voltage	Open base	-150	V
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-6	A
I_{CM}	Collector current-peak		-10	A
P_C	Collector power dissipation	$T_C=25$	80	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-65~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-150			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-4A ; I _B =-0.4A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-4A ; V _{CE} =-5V			-1.8	V
I _{CBO}	Collector cut-off current	V _{CB} =-150V ; I _E =0			-50	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-3V ; I _C =0			-50	μA
h _{FE-1}	DC current gain	I _C =-1A ; V _{CE} =-5V	40		280	
h _{FE-2}	DC current gain	I _C =-4A ; V _{CE} =-5V	20			
f _T	Transition frequency	I _C =-0.5A ; V _{CE} =-5V		50		MHz

◆ h_{FE-1} Classifications

R	Q	P	O
40-80	60-120	90-180	140-280

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PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)