Silicon PNP Power Transistors 2SA1332

DESCRIPTION

・With TO-220Fa package
・High V_{CEO}

APPLICATIONS

・Power amplifier applications
・Driver stage amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

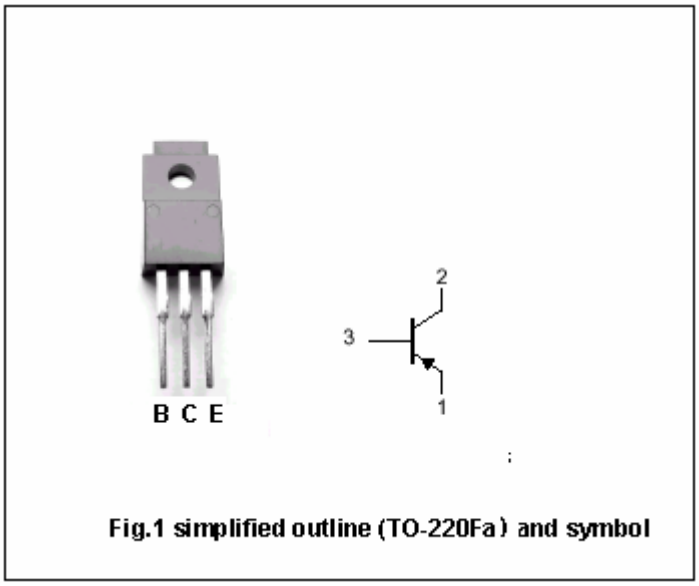

Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings(Ta=25℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-160	V
V_{CEO}	Collector-emitter voltage	Open base	-160	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-1.5	A
I_B	Base current		-0.15	A
P_C	Collector power dissipation	T_C=25℃	20	W
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-55~150	℃

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CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=10mA , I_B=0	-160			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=1mA , I_C=0	-5			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-0.5A, I_B=-50mA			-1.5	V
V_{BE}	Base-emitter voltage	I_C=-0.1A ; V_{CE}=-10V			-1.0	V
I_{CBO}	Collector cut-off current	V_{CB}=-160V, I_E=0			-1.0	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-5V; I_C=0			-1.0	μA
h_{FE}	DC current gain	I_C=-0.1A ; V_{CE}=-10V	60		240	
f_T	Transition frequency	I_C=-0.1A ; V_{CE}=-10V		200		MHz

PACKAGE OUTLINE

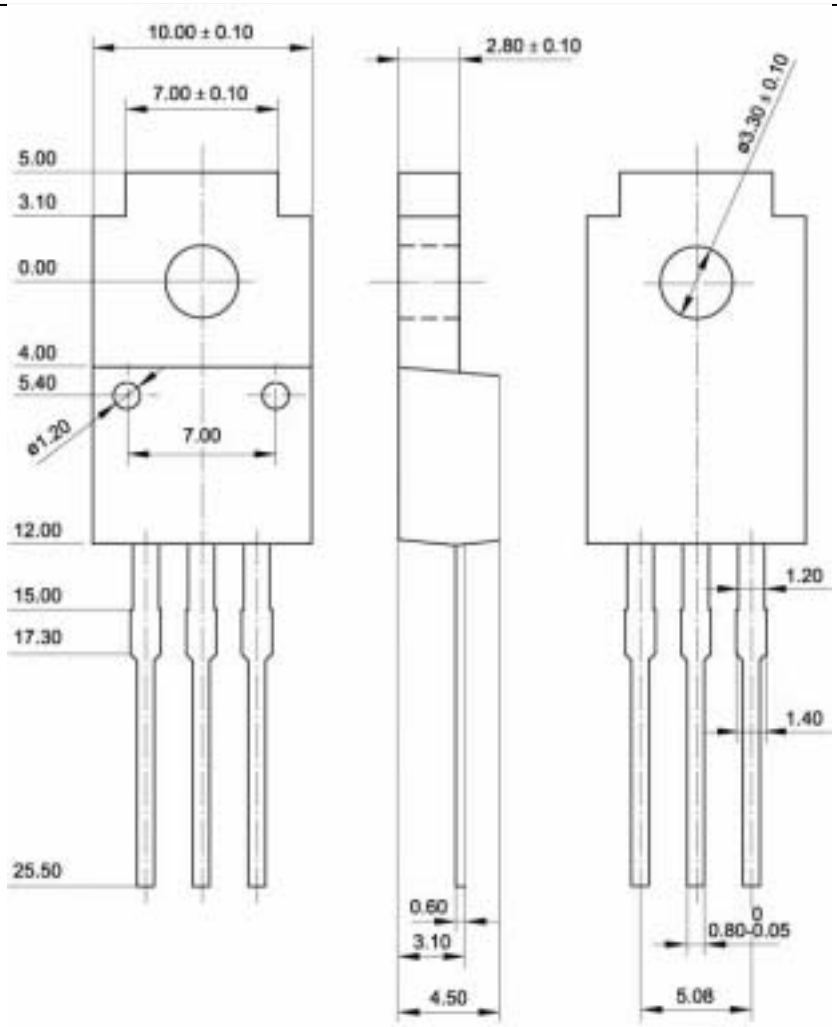

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)