

Silicon PNP Power Transistors

2SA1513

DESCRIPTION

- With TO-3PML package
- High current capability
- Low collector saturation voltage

APPLICATIONS

- For high speed and high power switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

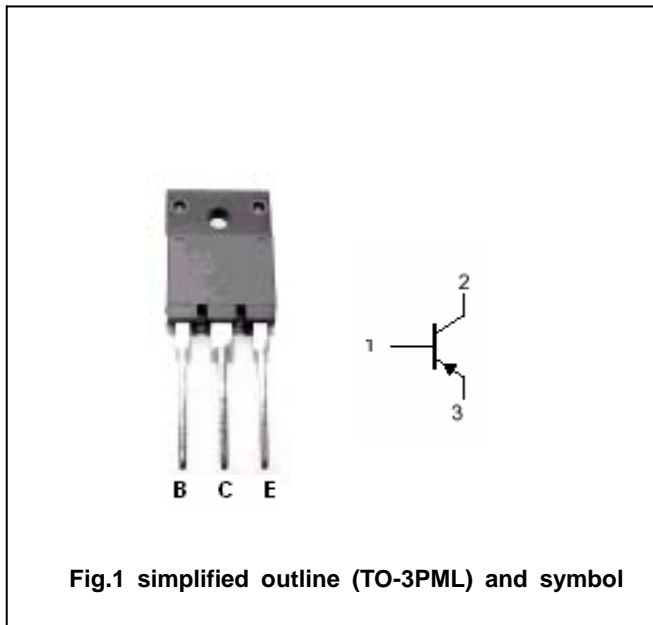


Fig.1 simplified outline (TO-3PML) and symbol

Maximum absolute ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector-emitter voltage	Open base	-60	V
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-15	A
P_C	Collector power dissipation	$T_a=25$	3.5	W
		$T_C=25$	60	
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA; I _B =0	-60			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA; I _C =0	-6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-12 A; I _B =-0.6 A			-0.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-12 A; I _B =-0.6 A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-60V; I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-6V; I _C =0			-10	μA
h _{FE}	DC current gain	I _C =-3A ; V _{CE} =-2V	100		400	
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-10V; f=1MHz		300		pF
f _T	Transition frequency	I _C =-1.5A ; V _{CE} =-10V		80		MHz

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PACKAGE OUTLINE

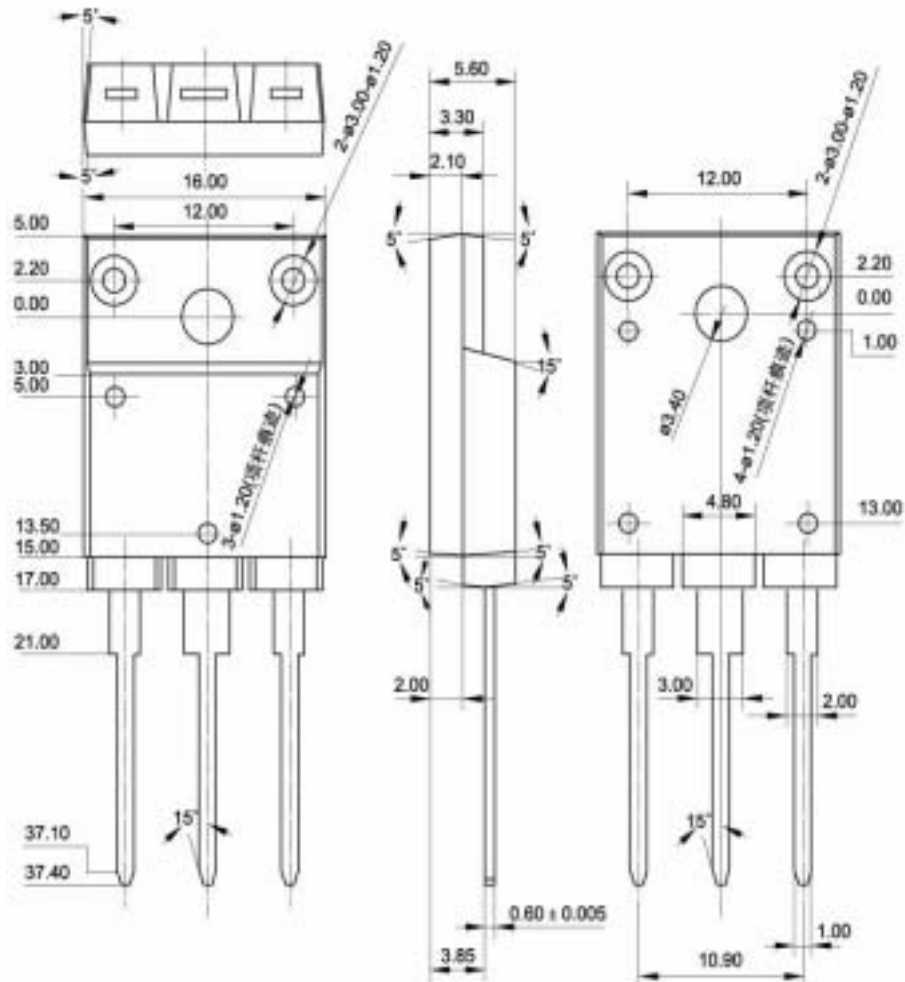


Fig.2 Outline dimensions