

Silicon NPN Power Transistors

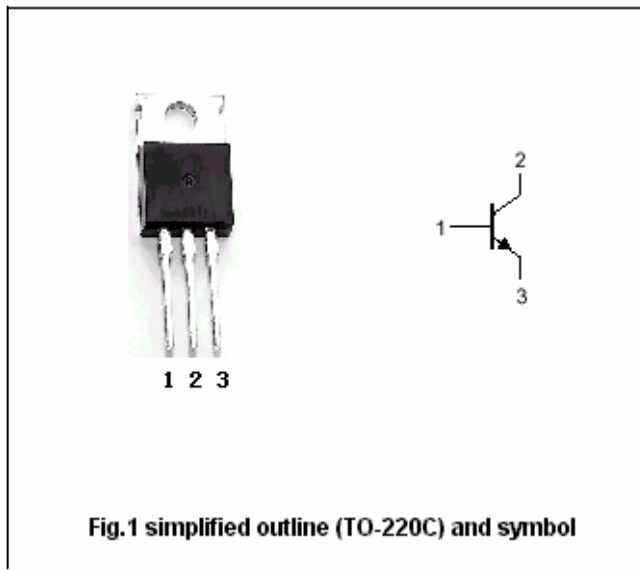
2SC3163

DESCRIPTION

- With TO-220C package
- High breakdown voltage
- High speed switching

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter



Absolute maximum ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	500	V
V_{CEO}	Collector-emitter voltage	Open base	400	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current		6	A
I_B	Base current		2	A
P_C	Collector dissipation	$T_C=25$	50	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
$R_{th j-C}$	Thermal resistance junction case	2.5	/W

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =100mA ; I _B =0	400			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =3A ; I _B =0.3A			1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =3A ; I _B =0.3A			1.5	V
I _{CEO}	Collector cut-off current	V _{CE} =400V ; I _B =0			100	μ A
I _{CBO}	Collector cut-off current	V _{CB} =500V ; I _E =0			100	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =7V ; I _C =0			100	μ A
h _{FE-1}	DC current gain	I _C =3A ; V _{CE} =2V	15			
h _{FE-2}	DC current gain	I _C =6A ; V _{CE} =2V	8			
f _T	Transition frequency	I _C =0.6A ; V _{CE} =10V		20		MHz

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PACKAGE OUTLINE



Fig.2 Outline dimensions (unindicated tolerance: ± 0.10 mm)