

**Silicon NPN Power Transistors**

**2SC5124**

**DESCRIPTION**

- With TO-3PML package
- High voltage switching transistor

**APPLICATIONS**

- Display horizontal deflection output
- Switching regulator and general purpose

**PINNING**

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

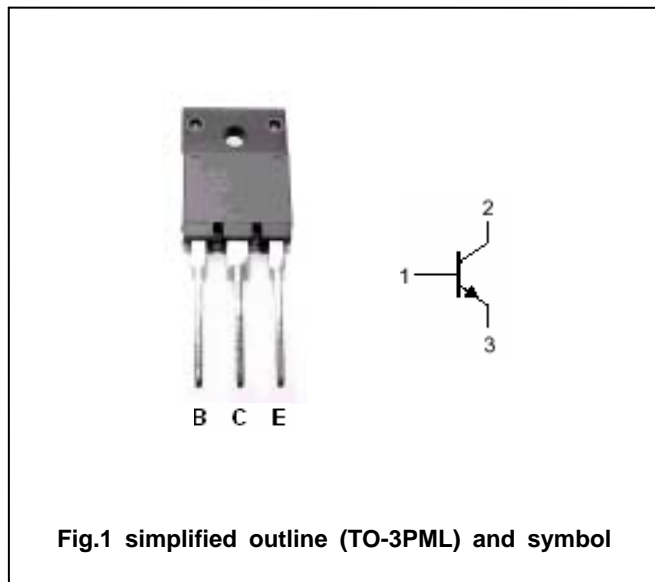


Fig.1 simplified outline (TO-3PML) and symbol

**Absolute maximum ratings(Ta=25 )**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	1500	V
$V_{CEO}$	Collector-emitter voltage	Open base	800	V
$V_{EBO}$	Emitter-base voltage	Open collector	6	V
$I_C$	Collector current		10	A
$I_{CM}$	Collector current-peak		20	A
$I_B$	Base current		5	A
$P_C$	Collector power dissipation	$T_C=25$	100	W
$T_j$	Junction temperature		150	
$T_{stg}$	Storage temperature		-55~150	

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =10mA; R <sub>BE</sub> =	800			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =8A; I <sub>B</sub> =2A			5	V
V <sub>BEsat</sub>	Base-emitter saturation voltage	I <sub>C</sub> =8A; I <sub>B</sub> =2A			1.5	V
I <sub>CBO1</sub>	Collector cut-off current	V <sub>CB</sub> =1200V; I <sub>E</sub> =0			100	μA
I <sub>CBO2</sub>	Collector cut-off current	V <sub>CB</sub> =1500V; I <sub>E</sub> =0			1	mA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =6V; I <sub>C</sub> =0			100	μA
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =1A; V <sub>CE</sub> =5V	8			
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =8A; V <sub>CE</sub> =5V	4		9	
f <sub>T</sub>	Transition frequency	I <sub>E</sub> =-1A; V <sub>CE</sub> =12V		3		MHz
C <sub>OB</sub>	Output capacitance	V <sub>CB</sub> =10V; f=1MHz		130		pF

## Switching times

t <sub>on</sub>	Turn-on time	I <sub>C</sub> =6A; I <sub>B1</sub> =1.2A; I <sub>B2</sub> =-2.4A R <sub>L</sub> =33.3 Ω; V <sub>CC</sub> =200V		0.1		μs
t <sub>stg</sub>	Storage time			4.0		μs
t <sub>f</sub>	Fall time			0.2		μs

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PACKAGE OUTLINE

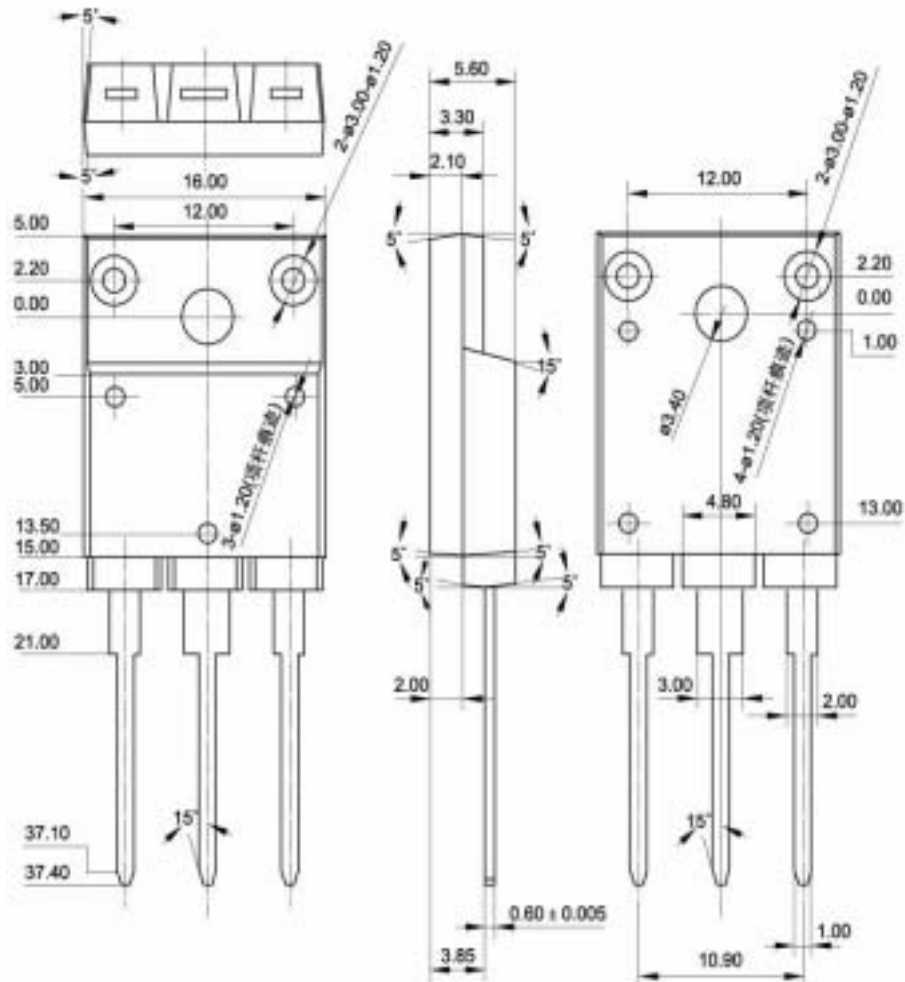


Fig.2 Outline dimensions

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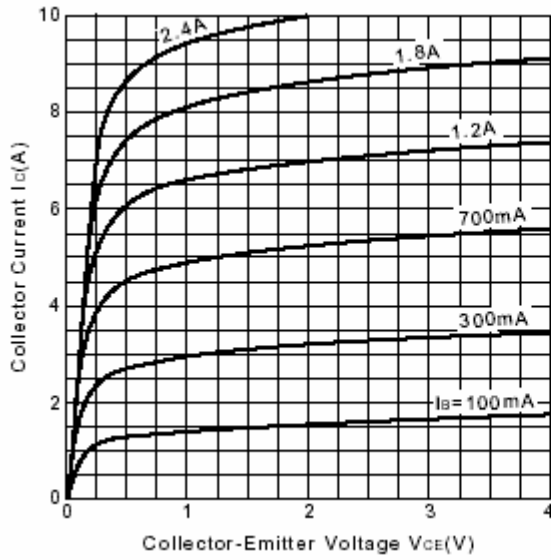


Fig.3 Static Characteristic

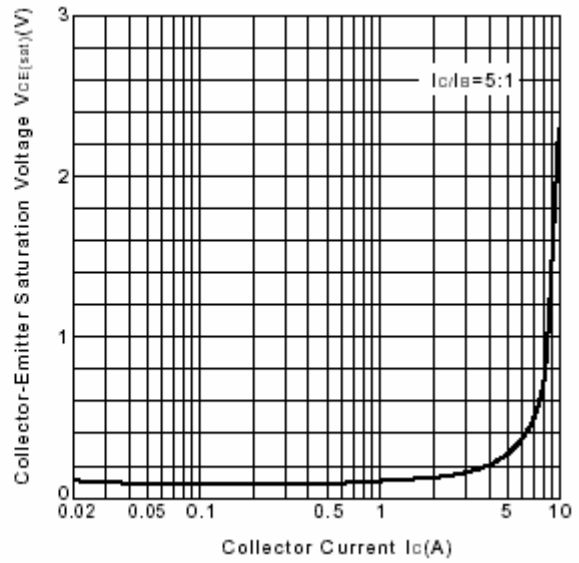


Fig.4  $V_{CE(sat)}$ - $I_c$  Characteristics

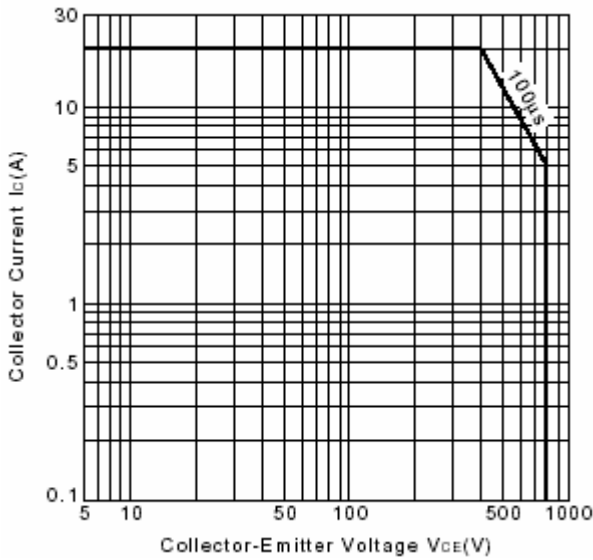


Fig.5 Safe Operating Area

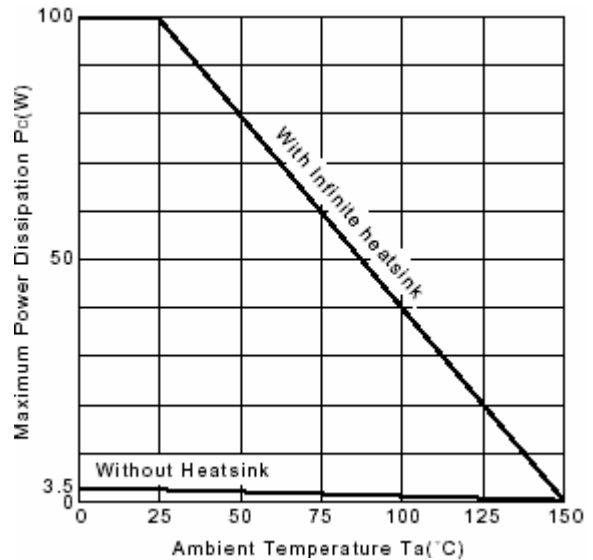


Fig.6  $P_c$ - $T_a$  Derating

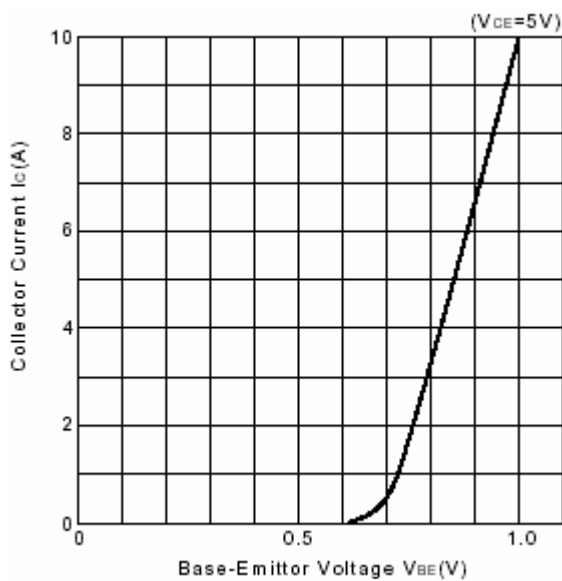


Fig.7  $I_c$ - $V_{BE}$

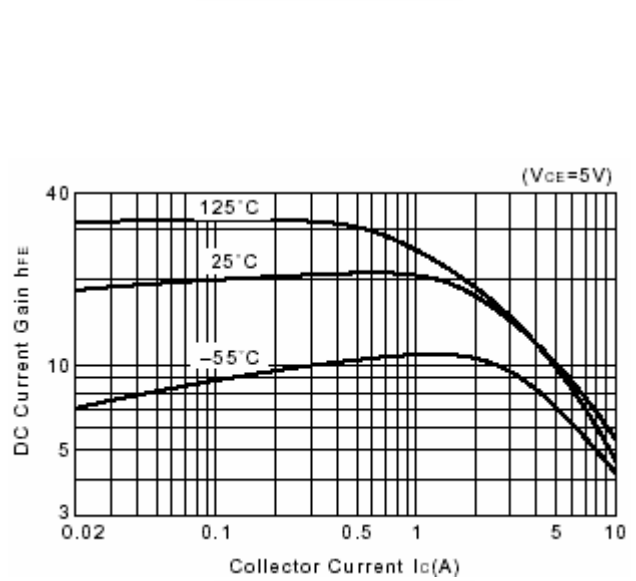


Fig.8 DC current Gain